Abdullah Fialah

Q1] Select the correct answer (**45 points, 3 points each**):

1) What is the number represented of the binary words 10010010, assuming the representation is in Two's complement
   A. -110
   B. 110
   C. -109
   D. -108
   E. None

2) The number $(161)_{10}$ is equivalent to:
   A. $(11)_{16}$
   B. $(1A)_{16}$
   C. $(A1)_{16}$
   D. $(AA)_{16}$
   E. None

3) The number $(55)_8$ is equivalent to:
   A. $(2D)_{16}$
   B. $(D2)_{16}$
   C. $(B1)_{16}$
   D. $(1B)_{16}$
   E. None

4) Using BCD code, when a computer adds $(01001001)_2 + (10000000)_2$ the result of this addition:
   A. is a correct BCD number.
   B. must be corrected by adding $(00000110)_2$.
   C. must be corrected by adding $(01100000)_2$.
   D. must be corrected by adding $(01100110)_2$.
   E. is wrong and can't be corrected.
   F. None

5) Even parity is:
   A. an extra bit added to make the total number of ones even to detect odd number of errors.
   B. an extra bit added to make the total number of ones even to detect even number of errors.

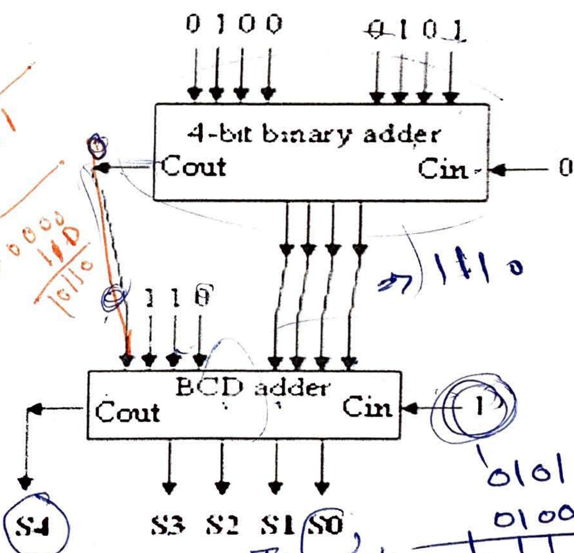
C. an extra bit added to make the total number of ones odd to detect odd number of errors.
D. an extra bit added to make the total number of ones odd to detect even number of errors.
E. an extra bit added to make the total number of ones even to detect any number of errors.

6) Given $F(x, y, z) = \prod(0, 3, 4, 7)$, and G is the complement of F, then:

A. $G(x, y, z) = \sum(0, 1, 2, 3, 5, 7)$
B. $G(x, y, z) = \prod(0, 3, 4, 7)$
C. $G(x, y, z) = \sum(1, 2, 5, 6)$
D. $G(x, y, z) = \sum(0, 3, 4, 7)$
E. None

7) The binary value of S4 S3 S2 S1 S0 in the circuit beside is

A. 1 0 0 0 1
B. 1 0 1 1 0
C. 1 0 0 0 0
D. 0 1 0 0 1
E. None



8) What is the result of Boolean expression simplification for $(B \oplus C) + (AB)'(A' + C')'$

A. $B \oplus C$
B. $A \oplus C$
C. $(B \oplus C)'$

D. $(A \oplus B)'$

E. None

9) In the shown K-map, the essential prime implicant is

A. AC

B. CD

C. A' D

D. A'C'

E. None

AB \ CD	00	01	11	10
00	1	X	1	X
01	1	X	1	
10			1	X
11			X	X

10) The output Y of the circuit computes

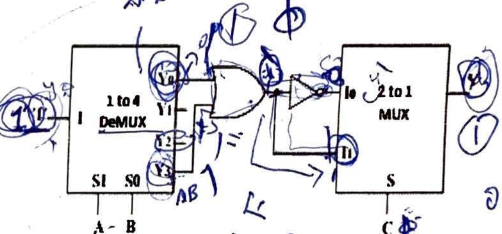
A. the sum bit of a full adder

B. the carry bit of a full adder

C. the complement of A

D. Complement of B

E. None



11. Which function F is implemented by using this 4X1 Multiplexer

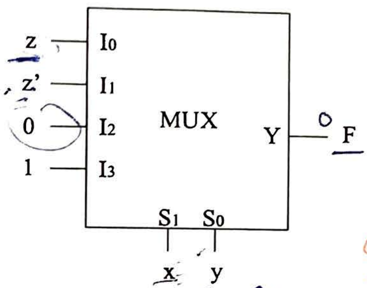
A. $F(x, y, z) = \sum(0, 3, 4, 5)$

B. $F(x, y, z) = \sum(1, 3, 6, 7)$

C. $F(x, y, z) = \sum(1, 2, 6, 7)$

D. $F(x, y, z) = \sum(1, 2, 5, 7)$

E. None



12. Implementation of full adder with two half adders and an ___ gate

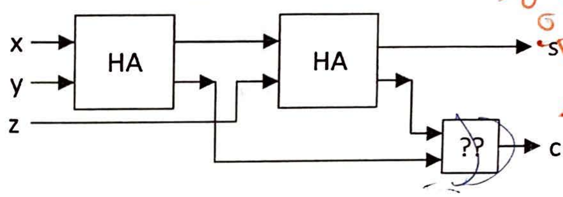
A. OR

B. NOR

C. XOR

D. XNOR

E. None



13. For the function F, the minimum product of sums expression

A. $F = w'x + w'y' + xy'z'$

B. $F = x'y + wx' + wz + wy$

C. $F = (x + y')(w' + x)(w' + z')(w' + y')$

D. $F = (w + x')\,(w + y)\,(x' + y + z)$

E. *None*

yz \ wx	00	01	11	10
00	1	1	1	
01	1	1		
11		1		
10		1		

14. For the shown Demux, the Boolean function is

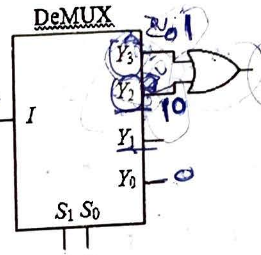
A. F = x' y' z + x y z

B. F = x' y z + x y z

C. F = x y' z + x y z

D. F = x y' z' + x y z

E. None



15. For the shown circuit the function F is

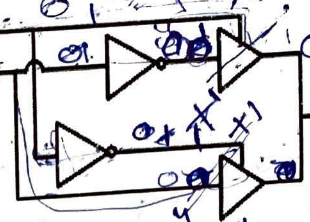
A. F = X AND Y

B. F = X OR Y

C. F = X XOR Y

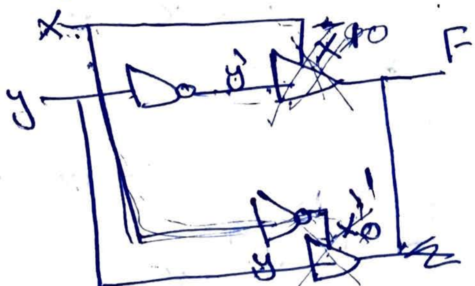
D. F = X XNOR Y

E. None



1	2	3	4	5	6	7	8	9	10
A	C	A	C	B	C	C	A	D	D

11	12	13	14	15
C	A	D	C	B



(2)

(0,1)	000-
(0,2)	00-0
(0,8)	-000
(1,3)	00-1
(1,5)	0-01
(2,3)	001-
(2,10)	-010
(8,10)	10-0
(3,7)	0-11
(5,7)	01-1
(10,14)	1-10
(7,15)	-111
(14,15)	111-

$PI_1 \Leftarrow$ (1,5)
$PI_2 \Leftarrow$ (3,7)
$PI_3 \Leftarrow$ (10,14)
$PI_4 \Leftarrow$ (7,15)
$PI_5 \Leftarrow$ (14,15)

(0,1,2,3)	00--
(0,2,1,3)	00--
(0,2,8,10)	-0-0
(0,8,2,10)	-0-0
(1,3,5,7)	0--1

PI_6 ← (0,1,2,3)
PI_7 ← (0,8,2,10)
PI_8 ← (1,3,5,7)

(3)

	0	1	2	3	5	7	8	10	14	15
PI_1		X			X					
PI_2				X		X				
PI_3								X	X	
PI_4						X				X
PI_5									X	X
PI_6	X	X	X	X						
PI_7	X		X				X	X		
PI_8		X		X	X	X				

P7 essential

$F = P_7 + P_0$ or P_1 or P_2 or P_3 or P_4 or P_5 or P_6

Q2] 18 points

Simplify using QM Tabulation method the following function

$$F(A,B,C,D) = \sum m(0,1,2,3,5,7,8,10,14,15)$$

0 = 0000 ✓
1 = 0001 ✓
2 = 0010 ✓
3 = 0011 ✓
5 = 0101 ✓
7 = 0111 ✓
8 = 1000 ✓
10 = 1010 ✓
14 = 1110
15 = 1111

(1)

✓0	0000	(0,1)	000-	(0,2,1,3)	00--
✓1	0001	✓(0,2)	00-0	(0,1,2,3)	00--
✓2	0010	✓(0,8)	-000	(0,2,8,10)	-0-0
✓8	1000			(0,8,2,10)	-0-0
✓3	0011	✓(1,3)	00-1	(1,3,5,7)	0--1
✓5	0101	(1,5)	0-01	(2,3,5,7)	0--1
✓10	1010	✓(2,3)	001-		
		✓(2,10)	-010		
		✓(8,10)	10-0		
✓7	0111	✓(3,7)	0-11		
✓14	1110	(5,7)	01-1		
		(10,14)	1-10		
15	1111	(7,15)	-111		
		(14,15)	111-		

(5)

PI1 = 000- (0,1)
PI2 = 0-01 (1,5)
PI3 = 01-1 (5,7)
PI4 = 1-10 (10,14)
PI5 = -111 (7,15)
PI6 = 111- (14,15)

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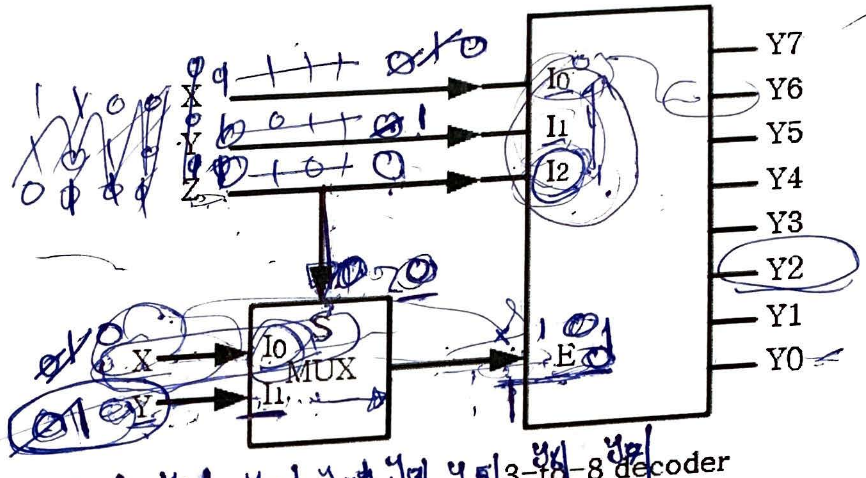
11

Q3] 12 points

For the shown logic diagram, determine for each input combination of X, Y and Z the value of each output, Y7 through Y0.



	x	y	z	y0	y1	y2	y3	y4	y5	y6	y7
0	0	0	0	0	0	0	0	0	0	0	0
1	0	0	1	0	0	0	0	0	0	0	0
2	0	1	0	0	0	0	1	0	0	0	0
3	0	1	1	0	0	0	0	1	0	0	0
4	1	0	0	0	0	0	0	0	0	0	0
5	1	0	1	0	0	0	0	0	0	1	0
6	1	1	0	0	0	0	0	0	0	0	1
7	1	1	1	0	0	0	0	0	0		

2

Q4] 10 points

Many offices and buildings use combination locks to control entry. As the design engineer of the *Wonderful Door Security Company,* you are asked to implement a door security system by using a card reader. There **are four inputs to the card reader**: inputs X, Y, and Z are used to validate the correct door code and input V is used to check if the card reader is still valid. After the card reader is being read by the system, there **are three outputs** to this system: alarm (A), door open (D), and Error (E). Door (D) will only open when the decimal value of the binary inputs (x, y, z) is odd (عدد فردي) **AND** the card reader is valid. The Error (E) signal goes on when the code on the card is correct (i.e. decimal value equal to odd) but the card is no longer valid. Finally, the alarm (A) will trigger when the code is incorrect (i.e. decimal value equal to even). **Derive the truth table only**

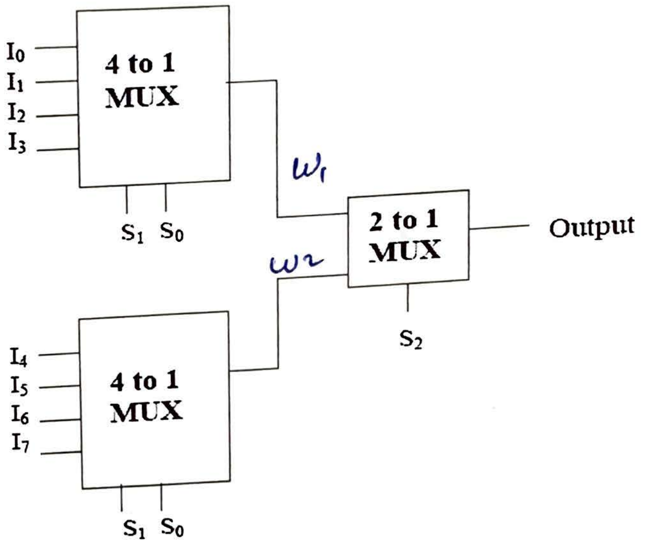
valid U=1
invalid U=0

	x	y	z	U	A (even)	D (عدد فردي valid)	E (عدد فردي)
0	0	0	0	0	1	0	0
1	0	0	0	1	0	1	0
2	0	0	1	0	1	0	0
3	0	0	1	1	0	1	0
4	0	1	0	0	1	0	0
5	0	1	0	1	0	1	0
6	0	1	1	0	1	0	0
7	0	1	1	1	0	1	0
8	1	0	0	0	1	0	0
9	1	0	0	1	0	1	0
10	1	0	1	0	1	0	0
11	1	0	1	1	0	1	0
12	1	1	0	0	1	0	0
13	1	1	0	1	0	1	0
14	1	1	1	0	1	0	0
15	1	1	1	1	0	1	0

D ⇒ odd and valid U=1
A ⇒ even
E ⇒ odd and invalid U=0

Q5] 15 points

For the system shown in the following figure



1. **(5 points)** Write a Verilog HDL code to describe the module mux4×1
2. **(4 points)** Write a Verilog HDL code to describe the module mux2×1
3. **(6 points)** Write a Verilog HDL code to describe the whole system structurally from its subsystems

(1)

```
module mux4x1 (I0, I1, I2, I3, S0, S1, w1)
  input I0, I1, I2, I3;
  output w1;
  reg w1;
  always @ (I0 or I1 or I2 or I3 or S0 or S1)
    if (S1==0 && S2==0)
      w1 = I0;
    else
    if (S1==0 && S2==1)
      w1 = I1;
    else
    if (S1==1 && S2==0)
      w1 = I2;
    else if (S1==1 && S2==1)
      w1 = I3;
endmodule
```

14

OK

(2)

```
module mux 2x1 (w1 ,w2 , S2, output)
  input w1 , w2 , S2 ;
  output output ;
  reg output ;
  always @ (w1 or w2 or S2)
    if (S2 = = 0)
      output = w1;
    else
     if (s = = 1)
      output = w2;

  end module;
```

OK

---

(3)

```
module System (I , S , w1, w2,output )
  input [7:0]I;
  input [2:0]S ;
  output w1 , w2;
  output output;

  mux4x1 M (I[0], I[1], I[2], I[3] , S[0], S[1], w1) ;
  mux4x1 M2 (I[4], I[5], I[6] , I[7], S[0], S[1], w2) ;
  mux 2x1 M3 (w1 , w2 , S[2] , output );

endmodule
```

OK